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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/591,890	09/07/2006	Claus Schmiederer	3765	7973

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EXAMINER	
THOMAS, LUCY M	

ART UNIT	PAPER NUMBER
2836	

MAIL DATE	DELIVERY MODE
01/16/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/591,890	SCHMIEDERER ET AL.	
	Examiner	Art Unit	
	Lucy Thomas	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeDaran et al. (US 2003/0048029) in view of Anthony (US 2003/0231451). Regarding Claim 1, DeDaran discloses an interference suppressor (see Figures 1, 3-5) for suppressing high-frequency interference emissions of a direct current motor 34 that is drivable in a plurality of stages and/or directions, having a plurality of capacitors 82, 84 (Figure 5) located on a first side (top side) of a printed circuit board 10 (Figure 1), 73 (Figure 4) and having a plurality of first conductor tracks 58, located on the first side of the printed circuit board, for putting the various capacitors into contact with a ground terminal 60, and having a first terminal (see terminal in Figure 5 to which one terminal of 82, and top terminal 74 of 72, and 16 are connected) and at least one second terminal (see terminal in Figure 5 to which one terminal of 84, and bottom terminal 76 of 72, and 18 are connected) for the individual stages of the direct current motor, the first terminal and the at least one second terminal being put into contact with a first connection line 38 for the first stage and at least one further connection line 40 for the at least one second stage of the direct current motor.

DeDaran does not specifically disclose that a ground face is located on a further side, diametrically opposite the first side, of the printed circuit board, and the first connection line and the at least one further connection line are fed through in insulated fashion relative to the ground face, and that the ground face is electrically connected via through-plated holes or via-holes.

Anthony discloses an interference suppressor 10 (see Figures) having plurality of capacitors 30, 32 arranged on a printed circuit board with metallized ground face 14 and with insulating apertures 18 for connection lines 12 to be fed through in an insulative fashion to the ground face (see Paragraphs 24, 76, 93), and wherein the ground face is electrically connected via through- plated holes or via-holes (thru-hole plating 2020 of apertures 2018 recited in Paragraph 109) to the ground terminals of the capacitors.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the surge suppressor of DeDaran with a ground face, because Anthony teaches the use metallized ground surface to provide a significantly large ground plane which helps with attenuation of radiated electromagnetic emissions and provides a greater surface area in which to dissipate over voltages and surges (see Anthony, Paragraph 75).

Regarding Claim 2, DeDaran discloses that at least one peak limiting devices/varistor and/or at least one capacitor 72 is located on the first side of the printed circuit board and is connected to the first terminal and the at least one further terminal, respectively, via second conductor tracks (see Paragraph 71).

Regarding Claim 3, DeDaran discloses that that the conductor tracks are located on the first side of the printed circuit board symmetrically about an axis of the printed circuit board (see Figures 1, 4). Regarding Claim 6, Anthony discloses that the through-plated holes are embodied as via-holes (thru-hole plating 2020 of apertures 2018 recited in Paragraph 109).

Regarding Claim 5, DeDaran discloses that the capacitors are embodied as SMD ceramic capacitors (Paragraph 57).

Regarding Claims 7-8, Anthony discloses a shielding housing (see enclosure or grounded chassis recited in Paragraph 76), surrounding the interference suppressor, which housing is connected electrically conductively to the ground face, and that the first connection line and the at least one second connection line are fed through the shielding housing (see Figure 1A).

Regarding Claim 12, DeDaran discloses that the capacitors and/or the at least one varistor and/or the at least one capacitor is contacted by way of radial or axial connection wires extended to the outside.

3. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeDaran et al. (US 2003/0048029) in view of Anthony (US 2003/0231451) and Migne (FR 2 783 369). Regarding Claim 9-10, DeDaran and Anthony do not specifically disclose that the shielding housing is connected electrically conductively to a motor housing of the direct current motor, via a plurality of contact points. Migne discloses a surge suppressor circuit on a printed circuit board for a DC motor, which is electrically conductively connected to a motor housing of the DC motor (see Abstract, Figures 1-4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of DeDaran and Anthony, and to have the shielding housing/carrier connection in a motor housing to reduce noise and spikes, because Magne teaches the use of such a connection in a DC motor.

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over DeDaran et al. (US 2003/0048029) in view of Anthony (US 2003/0231451) and Honl et al. (US 5,299,088). Regarding Claim 11, DeDaran and Anthony do not disclose that at defined points, the conductor tracks have tapered portions for a short- circuit guard. Honl discloses a protective circuit wherein conductor tracks 63, 65 have tapered portions 70, 71 for short circuit protection (see Figure 7, Column 7, lines 45-50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of DeDaran and Anthony, and to provide tapered or narrow portions on the conductive tracks for short circuit protection as taught by Honl, because tapered portions in the conductive tracks provide short circuit protection by forming fuse regions between the tracks and ground (see Honl, Column 7, lines 45-50).

Response to Arguments

5. Applicant's arguments filed 11/07/2008 have been fully considered.

6. Regarding Anthony reference, the Applicant argues that the reference neither shows nor suggests that a ground face of a printed surface board is electrically connected via through-plated holes or via-holes to the ground terminal of a capacitor.

Examiner respectfully disagrees. In Paragraph 93, Anthony references teaches “various conductive electrodes and common conductive plates, chassis and board noise

blocking capacitors are formed by the interaction of common ground conductive plates 112 and blocking electrodes 682 and 684. For instance, chassis is connected to the electrical conductors 1 and 7, both of which are electrically connected through coupling apertures 120.." See also Paragraphs 24, 76, 109 of Anthony. The thru-hole plating 2020 allows conductors 2034 and conductive pads 2024 adhering to the thru-hole plating, and at least one of the conductors or conductive electrodes 2034 has connection to ground surface to dissipates interferences or over voltages (see also reciting of Paragraph 93 above).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mizumoto et al. (US 5, 883, 335) discloses printed circuit board with via-holes for wiring connections.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lucy Thomas whose telephone number is 571-272-6002. The examiner can normally be reached on Monday - Friday 8:00 AM - 4:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/L. T./
Examiner, Art Unit 2836
January 07, 2009

/Stephen W Jackson/
Primary Examiner, Art Unit 2836